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(71) Applicant: FUJITSU LIMITED
1015, Kamikodanaka Nakahara-ku
Kawasaki-shi Kanagawa 211 (JP)

(72) Inventor: Yamashita, Koichi
1-8-3, Kurihira Asao-ku
Kawasaki-shi Kanagawa 215 (JP)

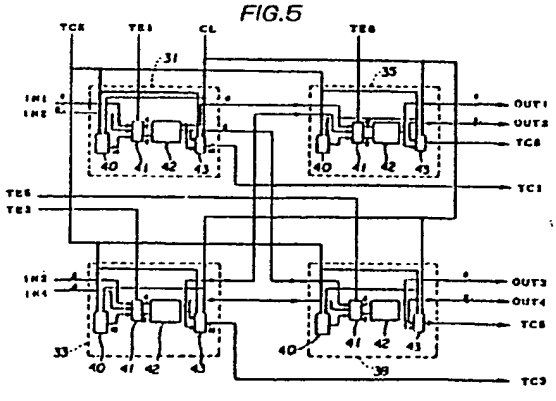
(74) Representative: Joly, Jean-Jacques et al
CABINET BEAU DE LOMENIE 55, rue d'Amsterdam
F-75008 Paris (FR)

The title of the invention has been amended (Guidelines for Examination in the EPO, A-III, 7.3).

(54) Semiconductor integrated circuit with a test function.

(57) A semiconductor integrated circuit comprises a plurality of integrated circuit blocks (31 - 39) constituted on a wafer (30), the integrated circuit blocks being arbitrarily electrically connected to each other so as to form a system. Each of the integrated circuit blocks comprises a logical operating circuit (42) for carrying out a logical operation; a pseudo-random pattern generating circuit (40) for generating a pseudo-random pattern signal; switching circuit (41) for selecting either an input signal to be processed by the logical operating circuit or the pseudo-random pattern signal in response to a test enabling signal (TE1 - TE9) which is independently applied to each integrated circuit block so that each integrated circuit block is independently set to either a test mode or a normal mode and for outputting the selected signal to the logical operating circuit; and a data compressing circuit (43) for compressing an output data signal of the logical operating circuit.

FIG.5



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the blocks 31 and 33 are passed through the switching circuits 40 and fed to the butterfly processors 42 in the blocks 35 and 38. Then, the output signals of the processors 42 are fed to the data compressors 43. Even when the blocks 35 and 38 are in the normal operating mode, the generator 40 and the compressor 43 are active.

Next, the test clock signal TCK is activated as shown in FIG.6(D). Then, the pseudo-random pattern generator 40 and the data compressor 43 of each block start to operate. Since the blocks 31 and 33 are maintained in the test mode, the pseudo-random pattern signals from the generators 40 thereof are passed through the switching circuits 41 and fed to the butterfly processors 42. The output signals of the butterfly processors 42 of the blocks 31 and 33 are fed to the integrated circuit blocks 35 and 38. The signals from the blocks 31 and 33 are passed through the switching circuits 41 of the blocks 35 and 38, respectively, and fed to the butterfly processors 42 thereof. Then, the output signals of the processors 42 of the blocks 35 and 38 are delivered to the data compressors 43 thereof, so that the compressed data (signature outputs) TC5 and TC8 are outputted through the output terminals (not shown) to the test device.

After a predetermined number of the test clock signal TCK is applied to the system, the compressed data derived from the blocks 35 and 38 are compared with an expected value data. If the system is not defective, both the data are identical to each other. In this way, it is possible to check the operation of the system by using the self-testing circuits each composed of the pseudo-random pattern generator and the data compressor built-in the integrated circuit blocks. Therefore, the additional self-testing circuit for the system test provided on the wafer is no longer necessary to check the operation of the system.

FIG.7 is a circuit diagram of the pseudo-random pattern generator 40 shown in FIG.5. As shown, the generator 40 consists of 15 delayed flip-flop circuits F1 to F15 with clear terminals, 1 delayed flip-flop F16 with a set terminal, and 3 exclusive-OR circuits E-OR. For simplicity, the test clock signal TCK and the clear signal CL are not illustrated. The pseudo-random pattern of 16 bits t1 to t16 is obtained at the output terminals of the flip-flop circuits F1 to F16. The structure shown in FIG.7 is so-called a linear feedback shift register producing a cyclic redundancy check signal.

FIG.8 is a detailed block diagram of the switching circuit 41. The switching circuit 41 is composed of sixteen 1-bit switching circuits illustrated with rectangular blocks. Symbols a1 to a16 denote bits of the input signal. Input bits of the switching circuit 41 are represented by i1 to i16.

FIG.9 is a circuit diagram of one 1-bit switching circuit. The 1-bit input signal a1 and 1-bit pattern signal t1 are inverted by inverters 41a and 41b and fed to transmission gates 41f and 41g, respectively. Tne transmission gates 41f and 41g are controlled by both the test enabling signal TE1 and an inverted test enabling signal. When one of the gates is in a closed state, the other is in an open state. The output signals of the gates 41f and 41g are inverted by an inverter 41d and fed to the butterfly processor 42.

FIG.10 is a circuit diagram of the data compressor 43. As illustrated, the data compressor 43 consists of 16 delayed flip-flop circuits F1 to F16 with clear terminals and 19 exclusive-OR circuits E-OR. For simplicity, the test clock signal TCK and the clear signal CL are not shown. Symbols tc1 to tc16 denote bits of the compressed data.

The present invention is not limited to the embodiment described in the foregoing, but various variations and modifications may be made without departing the scope of the present invention. For example, the present invention is not limited to the butterfly processor. Any logical operation for the integrated circuit block is applicable. The system may be constituted with combinations of the same kind of the integrated circuit blocks or different kinds of the integrated circuit blocks. Moreover, even when a plurality of systems are constituted in the semiconductor integrated circuit, these systems may be tested in the same manner as that described in the foregoing.

Claims

1. A semiconductor integrated circuit including a plurality of integrated circuit blocks (31 - 39) constituted on a wafer (30), said integrated circuit blocks being arbitrarily electrically connected to each other so as to form a system, each of said integrated circuit blocks comprising logical operating means (42) for carrying out a logical operation; pseudo-random pattern generating means (40) for generating a pseudo-random pattern signal; and data compressing means (43) for compressing an output data signal of said logical operating means, characterized in that each of said integrated circuit blocks further comprises switching means (41) for selecting either an input signal to be processed by said logical operating means or said pseudo-random pattern signal in response to a test enabling signal (TE1 - TE9) which is independently applied to each integrated circuit block so that each integrated circuit block is independently set to either a test mode or a normal operating mode, and for outputting the selected signal to said logical operating means.

2. A semiconductor integrated circuit as claimed in claim 1, characterized in that at the time of testing said system, said switching means of each of integrated circuit blocks (31, 33) positioned at first stage of said system is controlled by the test enabling signal so as to select the pseudo-random pattern, and said switching means of each of integrated circuit blocks (35, 38) other than the blocks at the first stage is controlled by the test enabling signal so as to select the input signals.

3. A semiconductor integrated circuit as

FIG. 1 (PRIOR ART)

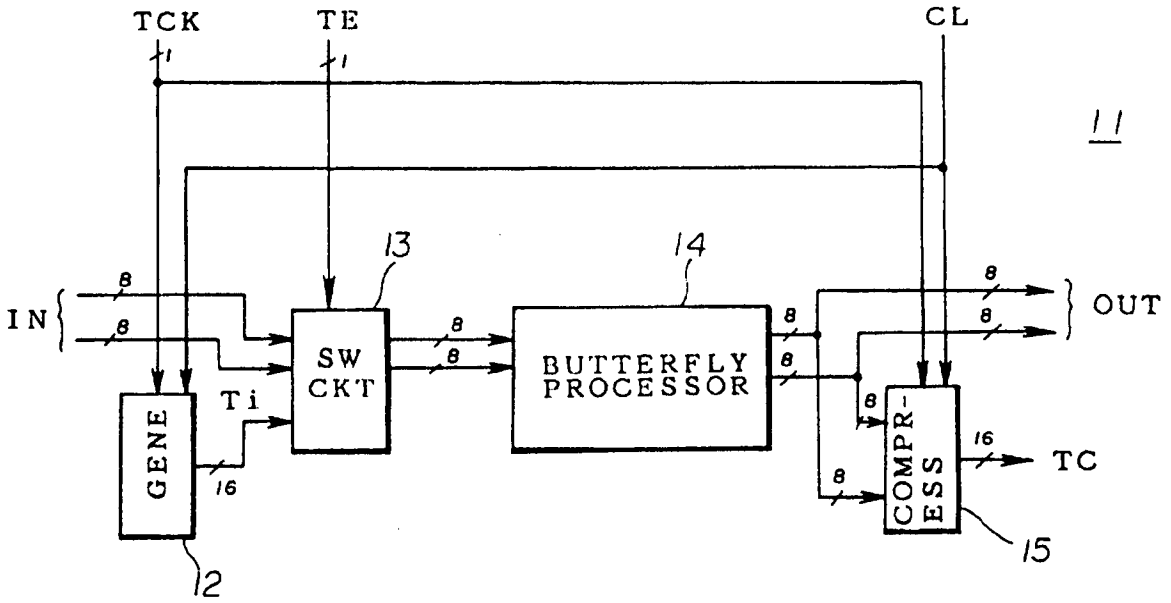

FIG. 2 (PRIOR ART)

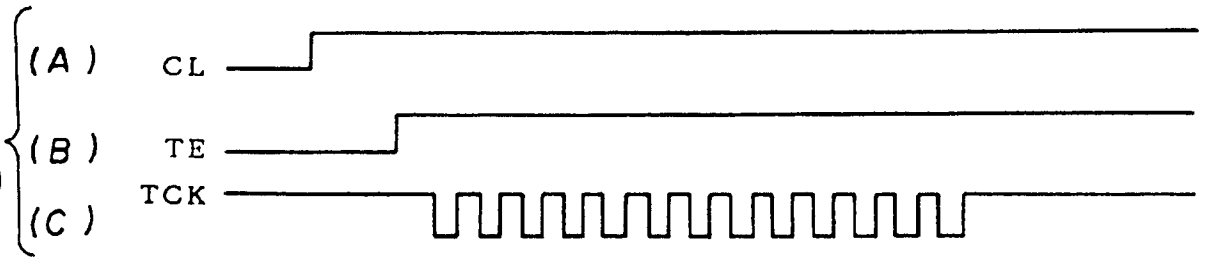

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FIG. 3A (PRIOR ART)

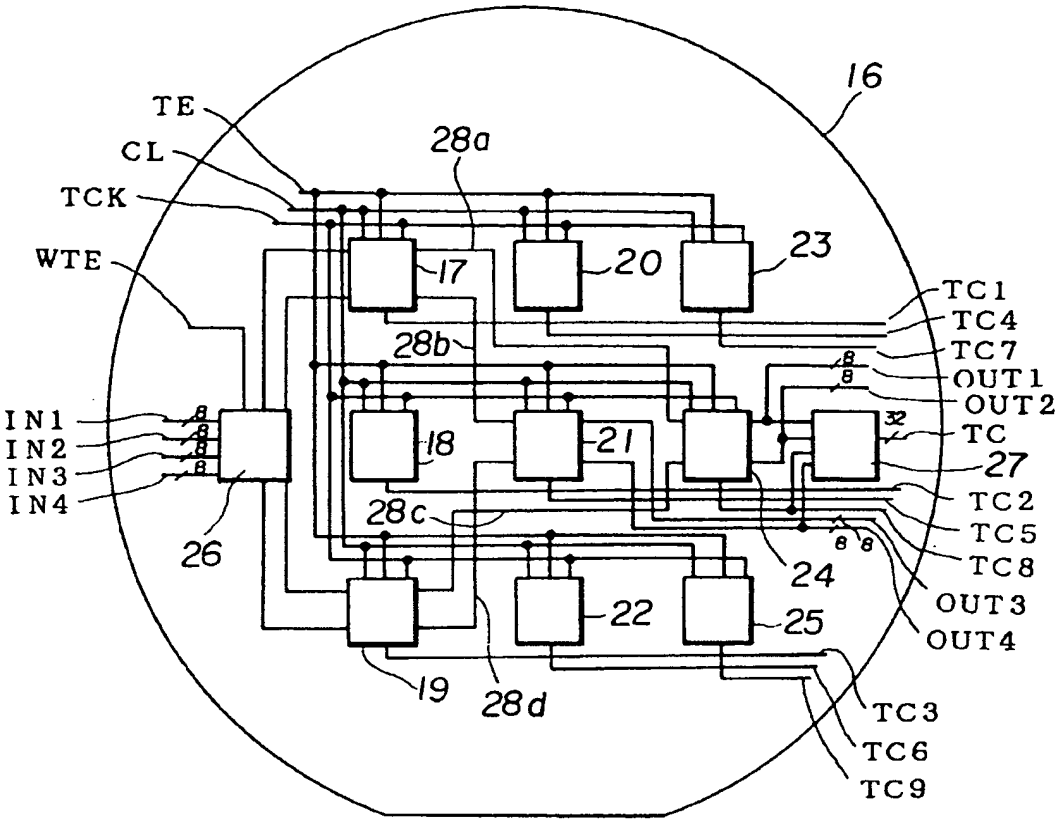


FIG. 3B (PRIOR ART)

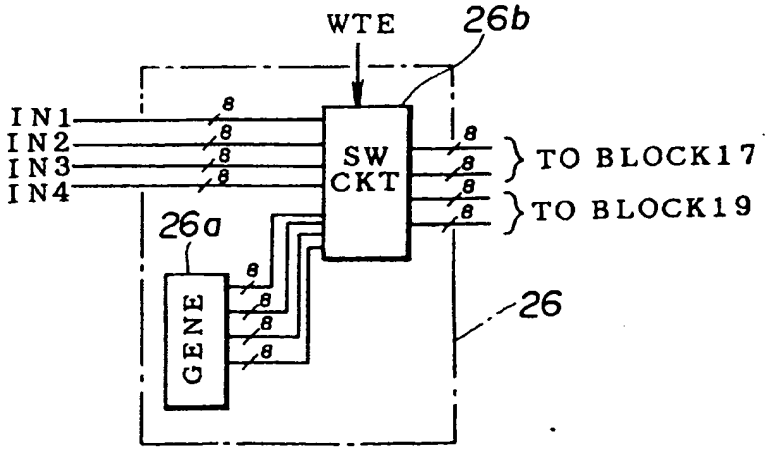


FIG.4

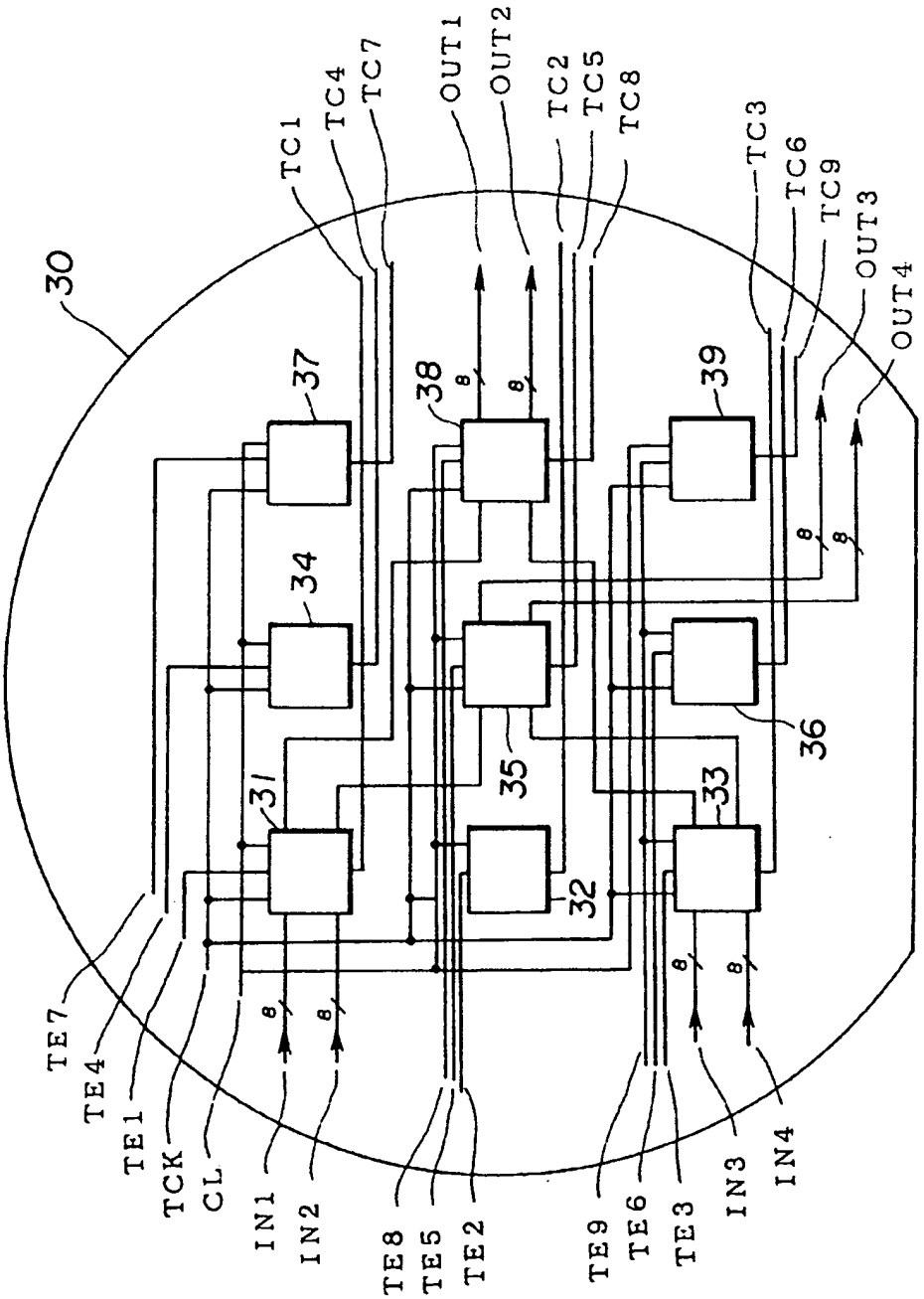

30
31
32
33
34
35
36
37
38
39
TC1
TC4
TC7
OUT1
OUT2
TC2
TC5
TC8
TC3
TC6
TC9
OUT3
OUT4
TE7
TE4
TE1
TCK
CL
IN1
IN2
TE8
TE5
TE2
TE9
TE6
TE3
IN3
IN4
8

FIG.5

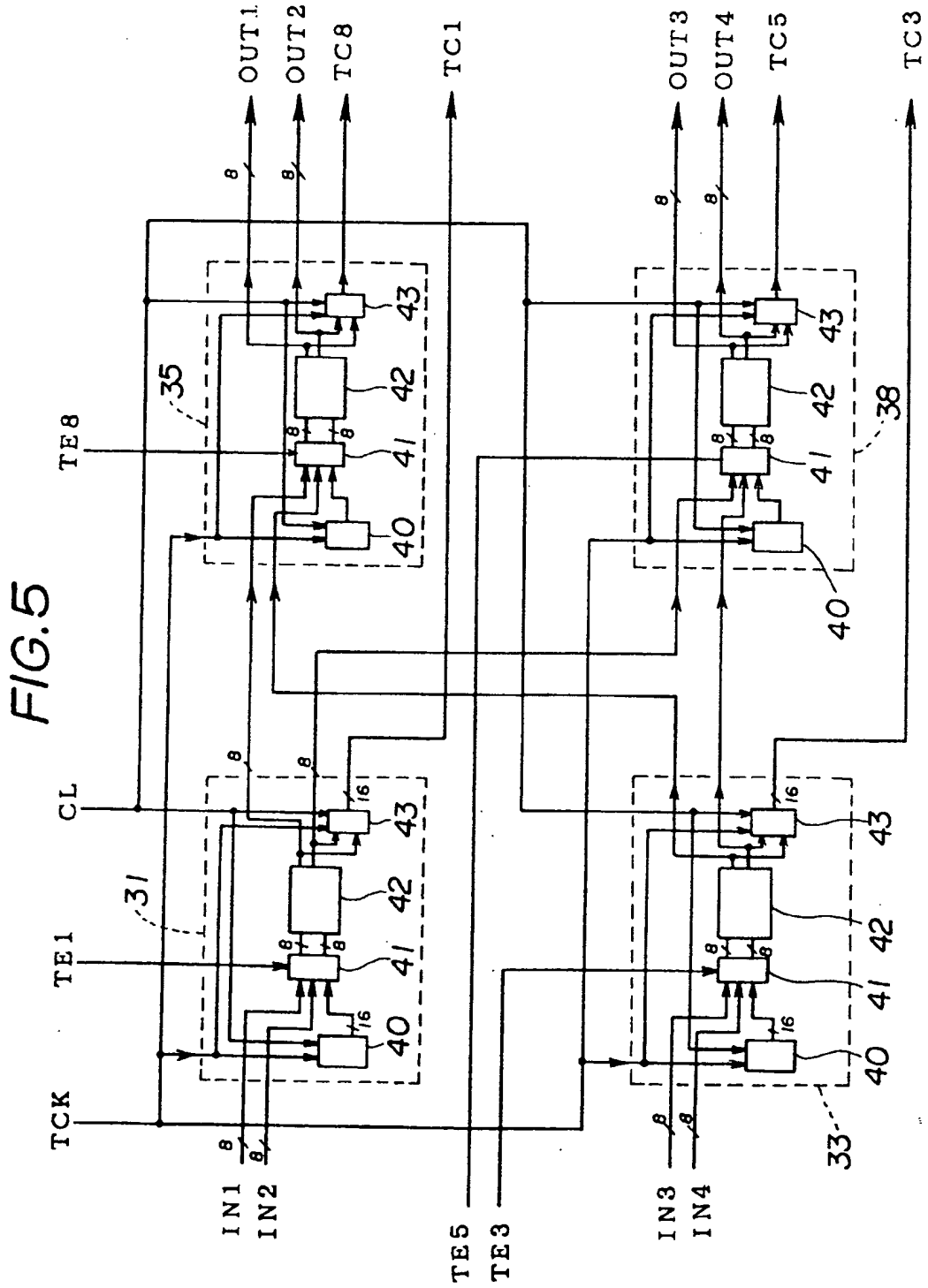

OUT1
OUT2
TC8
TC1
OUT3
OUT4
TC5
TC3
TE8
CL
TE1
TCK
IN1
IN2
TE5
TE3
IN3
IN4
35
31
38
33
40
41
42
43
8
16

FIG.6

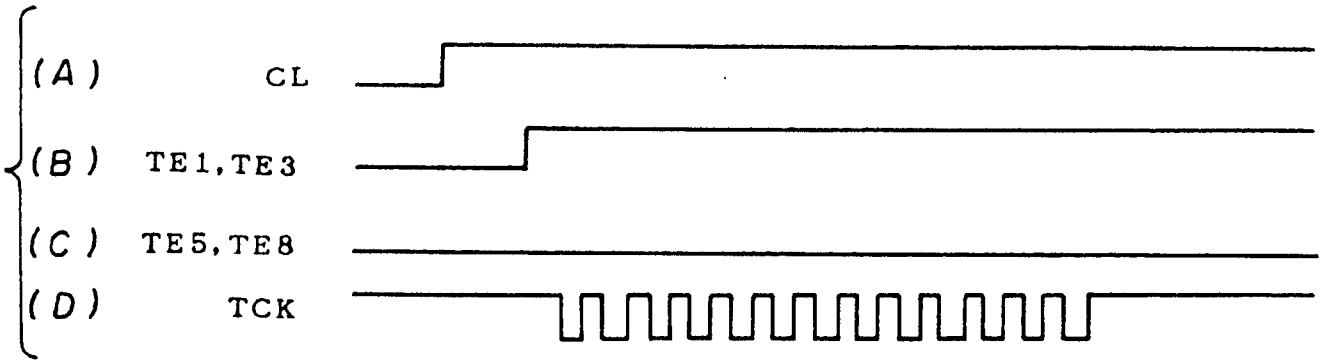


FIG.9

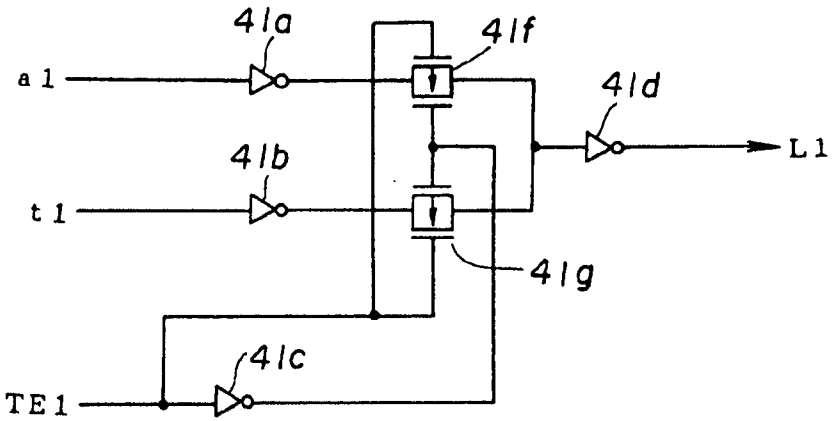


FIG. 7

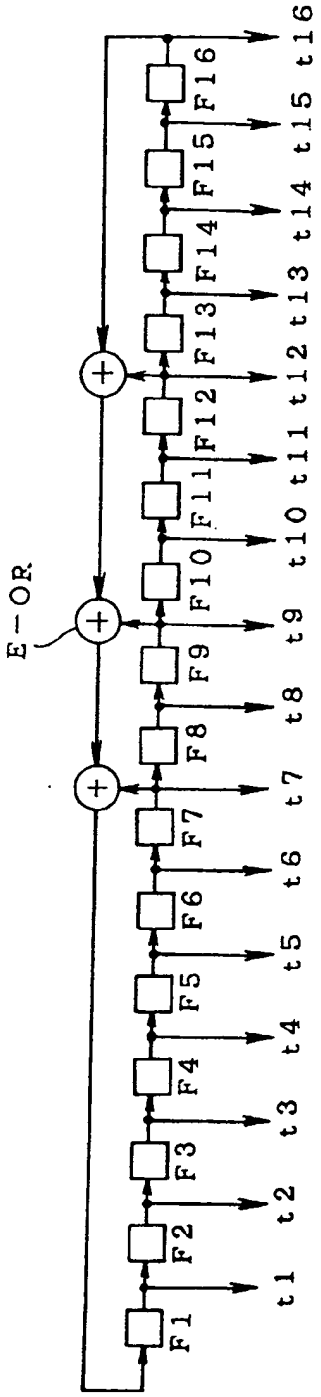

E-OR
F1
F2
F3
F4
F5
F6
F7
F8
F9
F10
F11
F12
F13
F14
F15
F16
t1 t2 t3 t4 t5 t6 t7 t8 t9 t10 t11 t12 t13 t14 t15 t16

FIG. 10

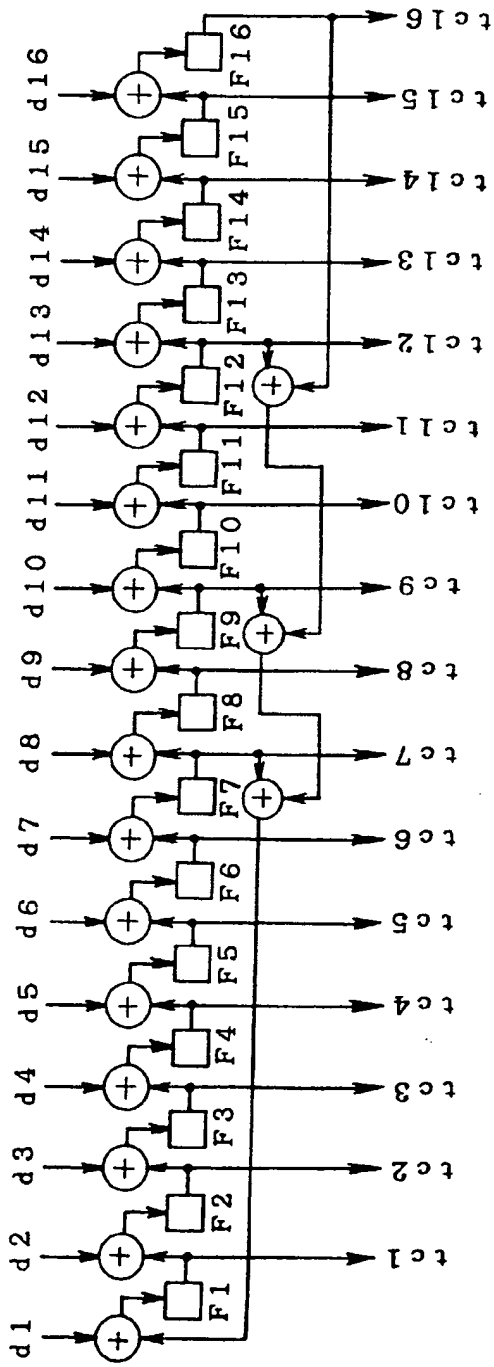
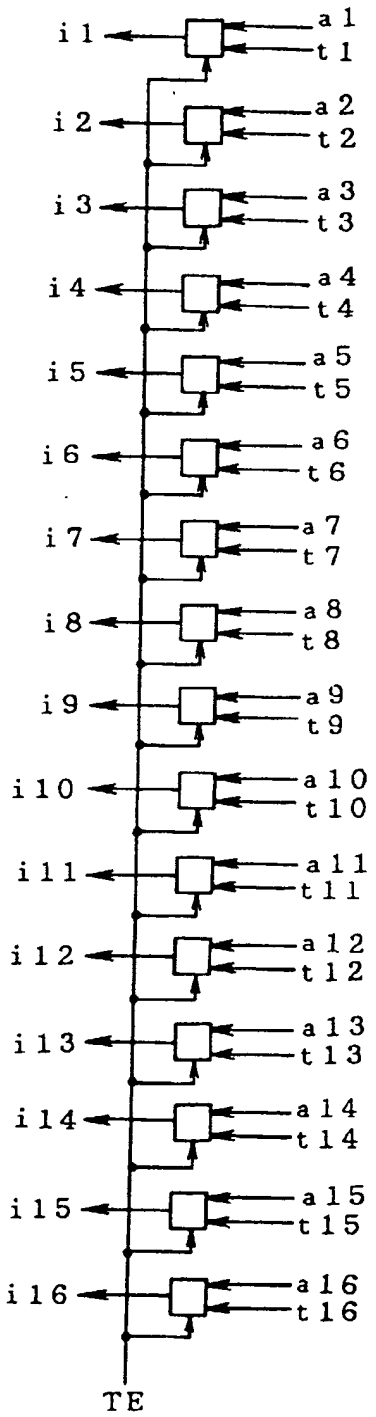

d1 d2 d3 d4 d5 d6 d7 d8 d9 d10 d11 d12 d13 d14 d15 d16
F1 F2 F3 F4 F5 F6 F7 F8 F9 F10 F11 F12 F13 F14 F15 F16
tc1 tc2 tc3 tc4 tc5 tc6 tc7 tc8 tc9 tc10 tc11 tc12 tc13 tc14 tc15 tc16

FIG.8


i 1
a 1
t 1
i 2
a 2
t 2
i 3
a 3
t 3
i 4
a 4
t 4
i 5
a 5
t 5
i 6
a 6
t 6
i 7
a 7
t 7
i 8
a 8
t 8
i 9
a 9
t 9
i 10
a 10
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(71) Applicant: FUJITSU LIMITED
1015, Kamikodanaka Nakahara-ku
Kawasaki-shi Kanagawa 211(JP)

(72) Inventor: Yamashita, Koichi
1-8-3, Kurihira Asao-ku
Kawasaki-shi Kanagawa 215(JP)

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CABINET BEAU DE LOMENIE 55, rue
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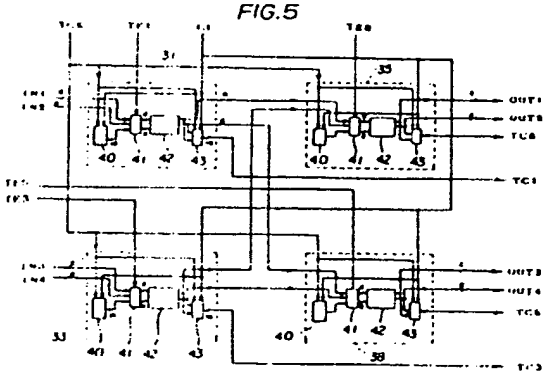

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European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 87 40 2872

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
Y	ELECTRONIC DESIGN, vol. 33, no. 16, 11th July 1985, pages 63-64, Schiphol, NL; M. BEEDIE: "Testing, fault tolerance emerge as top issues at wafer-scale conference" * Page 63, column 1, last paragraph - column 2; page 64, column 2, lines 39-46 *	1,3,4	G 01 R 31/28
A	* Page 63, column 3, lines 28-40 *	6	
Y	AUTOTESTCON'80-1980 AUTOTEST CONFERENCE, Washington, 2nd-5th November 1980, pages 135-139, IEEE, New York, US; D.K. BHAVSAR; "Self-testing supercells" * Page 138, paragraph "Polynomial division (POLYDIV) Scheme" *	1,3,4	
A	* Page 138, point "FSR" *	7	
P,X	PROCEEDINGS OF THE IEEE 1987 CUSTOM INTEGRATED CIRCUITS CONFERENCE, Portland, 4th-7th May 1987, pages 207-210, IEEE, New York, US; K. YAMASHITA et al.: "A wafer-scale 170,000-gate FFT processor with built-in test circuits" * Whole article *	1-7	

TECHNICAL FIELDS SEARCHED (Int. Cl.4)

G 06 F 11/26
G 01 R 31/28
G 06 F 11/20

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	12-12-1989	SARASUA GARCIA L.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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